

## Patent Claims

1. A semiconductor component comprising a stress-absorbing semiconductor layer, having:
  - 5 a carrier material (1);
  - a crystalline stress generator layer (SG) which is formed on the carrier material (1) and substantially has a first lattice constant, for generating a mechanical stress;
  - 10 an insulating stress transmission layer (2) which is formed on the stress generator layer (SG) and is used to transmit the mechanical stress which is generated;
  - a crystalline, stress-absorbing semiconductor layer (SA) which is formed on the stress transmission layer
  - 15 (2) and has a second lattice constant, which is different than the first lattice constant, for absorbing the mechanical stress which has been generated and transmitted and for realizing source/drain regions (S, D) and a channel region (K);
  - 20 a gate dielectric (3) which is formed at least at the surface of the channel region (K); and
  - a control layer (4) for driving the channel region (K), which is formed on the gate dielectric (3).
- 25 2. The semiconductor component as claimed in patent claim 1, wherein the stress-absorbing semiconductor layer (SA) has a thickness (d) less than  $1/3$  of a length (L) of the channel region (K).
- 30 3. The semiconductor component as claimed in patent claim 1 or 2, wherein the stress transmission layer (2) forms a crystalline insulator layer.
- 35 4. The semiconductor component as claimed in patent claim 3, wherein the stress transmission layer (2) has a lattice constant which is matched to the second lattice constant of the stress-absorbing semiconductor layer (SA).

5. The semiconductor component as claimed in one of patent claims 1 to 4, wherein the stress generator layer (SG) is an approx. 10 to 300 nm thick SiGe layer,  
5 the stress transmission layer (2) is an approx. 1 to 2 nm thick CaF<sub>2</sub> layer, and  
the stress-absorbing semiconductor layer (SA) is an approx. 5 nm thick Si layer.

10 6. The semiconductor component as claimed in one of patent claims 1 to 5, wherein the gate dielectric (3) has a high dielectric constant.

7. The semiconductor component as claimed in one of  
15 patent claims 1 to 6, wherein the control layer (4) includes a metal.

8. The semiconductor component as claimed in one of patent claims 1 to 7, wherein the carrier material (1)  
20 includes  
an Si substrate (1A) with a (100) surface orientation, and  
an Si buffer layer (1B) for generating a flat starting surface for the stress generator layer (SG).

25 9. A method for fabricating a semiconductor component with stress-absorbing semiconductor layer, comprising the steps of:

- a) forming a carrier material (1);
- 30 b) forming a crystalline stress generator layer (SG) having substantially a first lattice constant on the carrier material (1) in order to generate a mechanical stress;
- c) forming an insulating stress transmission layer  
35 (2) on the stress generator layer (SG) for transmitting the mechanical stress which has been generated;
- d) forming a crystalline, stress-absorbing semiconductor layer (SA) having a second lattice

constant, which is different than the first lattice constant, on the stress transmission layer (2) for the purpose of absorbing the mechanical stress;

- e) forming a gate dielectric (3) on the stress-absorbing semiconductor layer (SA);
- 5 f) forming a control layer (4) on the gate dielectric (3);
- g) patterning the gate dielectric (3) and the control layer (4); and
- 10 h) forming source/drain regions (S, D) in the stress-absorbing semiconductor layer (SA).

10. The method as claimed in patent claim 9, wherein in step a) a semiconductor substrate (1A) having a  
15 (100) surface orientation is provided, and a semiconductor buffer layer (1B) is epitaxially deposited thereon in order to produce a smooth surface.

11. The method as claimed in patent claim 9 or 10,  
20 wherein in step b) a IV-IV or III-V semiconductor is used.

12. The method as claimed in patent claim 11, wherein in step b) a multiple layer sequence is formed as  
25 stress generator layer (SG).

13. The method as claimed in one of patent claims 9 to 12, wherein in step b) the stress generator layer (SG) is smoothed by means of a molecular beam epitaxy  
30 process.

14. The method as claimed in one of patent claims 9 to 13, wherein in step c) a crystalline insulator layer is formed as stress transmission layer (2).

35 15. The method as claimed in patent claim 14, wherein in step c) a stress transmission layer (2) with a lattice constant which is matched to the second lattice

constant of the stress-absorbing semiconductor layer (SA) is formed.

16. The method as claimed in patent claim 15, wherein  
5 in step c) only a few atom layers of the stress transmission layer are deposited epitaxially on the stress generator layer (SG).

17. The method as claimed in one of patent claims 9 to  
10 16, wherein in step d) a fully depleted semiconductor material is used.

18. The method as claimed in one of patent claims 9 to  
15 17, wherein in step e) a material with a high dielectric constant is used as gate dielectric (3).

19. The method as claimed in one of patent claims 9 to  
20 18, wherein in step f) a metal is used as control layer (4).

20. The method as claimed in one of patent claims 9 to  
19, wherein  
in step a) Si is used as carrier material (1);  
in step b) SiGe is used as stress generator layer (SG);  
25 in step c)  $\text{CaF}_2$  is used as stress transmission layer (2);  
in step d) Si is used as stress-absorbing semiconductor layer (SA);  
in step e)  $\text{HfO}_2$  is used as gate dielectric (3); and  
30 in step f) TiN is used as control layer (4).